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(71) Applicant: MOTOROLA, INC. [US/US]; 1303 East Algonquin Road, Schaumburg, IL 60196 (US).

(72) Inventor: LAFLIN, Timothy, C. ; #9 Islington Place, Boynton Beach, FL 33462 (US).

(74) Agents: INGRASSIA, Vincent, B. et al.; Motorola, Inc., Intellectual Property Dept., 1500 N.W. 22nd Avenue, Boynton Beach, FL 33426-8753 (US).

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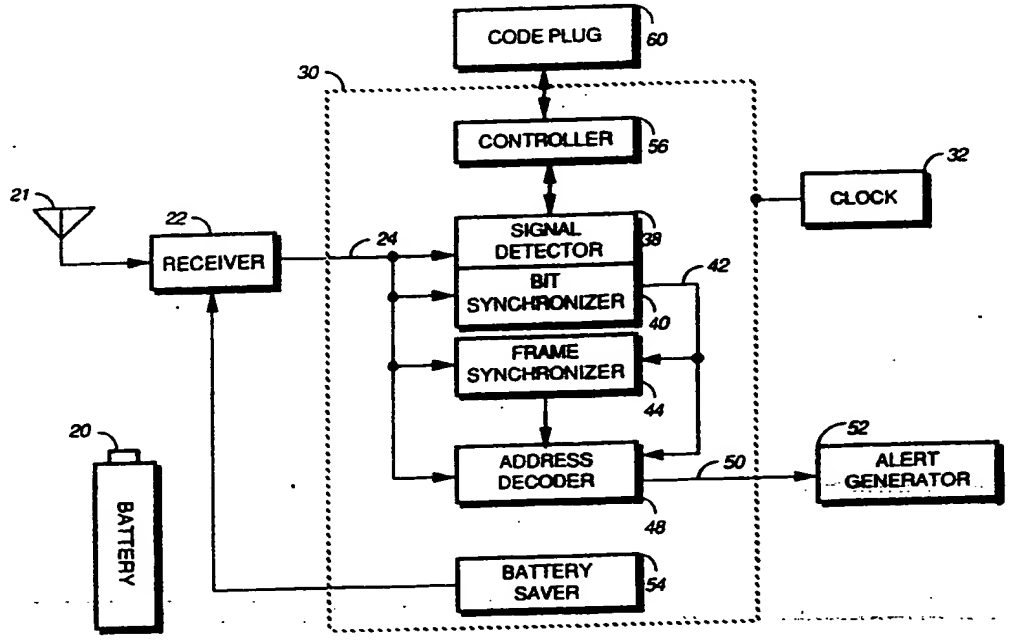

(57) Abstract

A receiver (22) capable of receiving a plurality of signals, wherein more of the signals are received at a peak time than at an off peak time, comprises first circuitry (38) for determining if the signals are being received by searching in a first search mode and second circuitry (38) for determining if the signals are not being received by searching in a second search mode. Selection circuitry (56) activates the first means during the peak time and activates the second means during the off peak time. The first and second search modes comprise searching for the signal and searching for noise, respectively.

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TIME BASED SIGNAL DETECTOR

Field of the Invention

This invention relates in general to a data receiver that synchronizes received data transmissions, and more particularly to a signal detector and bit synchronizer for use in a portable selective call receiver that performs a signal search in a selectable one of two or more modes depending on the time of day.

Background of the Invention

Bit synchronization to a digital transmission is a process used to determine the presence of symbol boundaries of a data transmission and thereafter to optionally provide a bit clock to synchronously sample data bits, or data symbols from the data transmission. Bit synchronization may be a process used in a selective call receiver decoding a digital signaling protocol, for example, that proposed by British Telecom in England which is commonly termed POCSAG (Post Office Code Standardization Advisory Group).

Synchronization to such a protocol is known and has been described in detail in U.S. Patent 4,518,961 which shows synchronization to either the POCSAG or a Golay signalling protocols. Additionally, U.S. Patent 4,506,262 shows synchronization to POCSAG using an early/late phase locked loop with course and fine synchronization modes.

Referring to FIG. 1, line 10 comprises a typical POCSAG signal. Prior to the signal, noise or another type of protocol may be transmitted as shown in area 12 enclosed in a broken line. The POCSAG signal begins with a preamble signal, 14, which comprises a number of one-zero transitions. The preamble is followed by a plurality of thirty two bit information words, each coded in a 31,21 extended BCH code (32,21). The information words begin with a sync code word 16a which contains predetermined binary sequence. Every seventeenth word thereafter another sync code 16b occurs in the signal. Between the sync codes, the information is structured as eight information frames each of which comprises two 32,21 words. For illustration, the contents of frame 4, as indicated by the number 18, is shown on line 34. Line 34 has two 32 bit words, 36 and 38, each information word having 32 data bits structured in

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the 32,21 format. It can be appreciated that the data bits shown on line 34 can appear to be effectively a random sequence.

The sync code provides a means for frame synchronization to the signal. Thus it is desirable to first bit synchronize to the preamble signal and subsequently frame synchronize to the sync code. Line 20 shows the operation of a selective call receiver synchronizing to the POCSAG signal. During interval 22 and 24, the selective call receiver is attempting to synchronize to the signal. However, the signal is not present. During interval 26, the preamble signal, 14, is present, the selective call receiver bit synchronizes and finds sync code 16a. Then in a known manner, the selective call receiver decodes information in preassigned frame 4 as shown by intervals 28 and 32. The selective call receiver also tests for sync code 16b during interval 30 in order to determine the continued presence of the transmission.

In some instances, the preamble signal may be corrupted by noise rendering the the preamble signal undetectable. In this situation, it is desirable to acquire bit synchronization on the data bits within the thirty two bit words, and subsequently frame synchronize to one of the periodic sync code signals. The bit synchronization process in this mode is more difficult because the data in the thirty two bit words is effectively random. Consequently, it is desirable to provide a selective call receiver capable of acquiring bit synchronization on either a POCSAG preamble signal or data signals within POCSAG information words.

Battery life is a critical aspect of portable selective call receivers and it is desirable to conserve battery power whenever possible. In the absence of the POCSAG signal, selective call receivers operate in a low power mode and periodically activate receiving and decoding circuitry in order to detect the presence of the POCSAG signal. If no signal is detected, the selective call receiver again operates in a low power mode. This process conserves battery power. Thus it is desirable to quickly detect the absence of the signal in order to hasten the return to the low power mode.

Prior art selective call receivers have typically analyzed a predetermined number of transitions and in response to various algorithms determine the absence of the POCSAG signal. One such algorithm is shown in U.S. Patent 4,554,665 wherein the using of a predetermined number of transitions requires waiting for all of the transitions to occur. Such techniques suffer greatly under conditions where transitions occur relatively infrequently, such as when low

frequency tones are transmitted in place of the POCSAG signal. While waiting for all of the transitions to occur, the prior art receivers are consuming additional battery power.

Furthermore, prior art selective call receivers typically establish a predetermined relationship between the sensitivity of detecting the POCSAG signal in a noise environment and falsely detecting a POCSAG signal when only noise or another signal is present. Since upon the detection of the absence of a POCSAG signal, power is conserved by deactivating the receiver, this establishment results in a certain average battery power consumption while searching for signal. However because selective call receivers are used in many different selective call receiver environments around the world, a sensitivity and falsing and battery power consumption performance in one application may not be optimal for another application.

Yet further, a recent version of the POCSAG signal has a 1200 baud data rate. Typical bit synchronizers capable of synchronizing to a data transmission having random data at 1200 baud will also synchronize to data transmissions being an integer divisor of that data rate (600, 300 baud). For example, the Golay Sequential Code (GSC) is another selective call receiver protocol which transmits message information at 600 and 300 baud.

Additionally, prior art selective call receivers with microcomputers typically sample the incoming signal at a very high rate, and typically use a digital phase locked loop implemented in software in order to establish a bit clock for sampling data bits after synchronization. Software generated digital phase locked loops require high sampling rates and continuous phase adjustments in a real time software environment. This requires a microcomputer to operate at a relative high bus rate. U.S. Patent 4,414,676 shows a synchronizer which samples at five times the data rate and performs numerous calculations between each sample; however, it does not show the capability to synchronize on random data.

Summary of the Invention

A receiver capable of receiving a plurality of signals, wherein more of the signals are received at a peak time than at an off peak time, comprises first circuitry for determining if the signals are being received by searching in a first search mode and second circuitry for determining if the signals are

not being received by searching in a second search mode. Selection circuitry activates the first means during the peak time and activates the second means during the off peak time.

Brief Description of the Drawings

FIG. 1 is a prior art implementation of the POCSAG signal and a selective call receiver's operation in response thereof.

FIG. 2 is a block diagram of a selective call receiver in accordance with an embodiment of the present invention.

FIG. 3 is a block diagram of a synchronizer operating in accordance with an embodiment of the present invention.

FIG. 4 shows signal detection and bit synchronization as a task operating in a multi-tasking program operating within the microcomputer operating within the selective call receiver.

FIG. 5 shows the operation of the signal search routine of FIG. 4.

FIG. 6 shows selecting the phase of the bit clock in response to the detection of the presence of the signal.

FIG. 7 illustrates the response of the signal detector to a strong signal.

FIG. 8 illustrates the response of the signal detector to a weak signal

FIG. 9 illustrates the response of the signal detector to the absence of a signal, or the presence of noise.

FIG. 10 illustrates the response of the signal detector to a strong signal having the desired baud rate.

FIG. 11 illustrates the response of the signal detector to a strong signal having the baud rate one half of the desired baud rate.

FIG. 12 is a table indicating the operation of the invention under conditions similar to those of FIG. 7.

FIG. 13 is a table indicating the operation of the invention under conditions similar to those of FIG. 8.

FIG. 14 is a table indicating the operation of the invention under conditions similar to those of FIG. 9.

FIG. 15 is a graph illustrating selective call receiver system loading versus the time of day.

FIG. 16 is a flowchart of a first embodiment which selects between the signal present and signal absent search modes.

FIG. 17 is a flowchart of a second embodiment which selects between the signal present and signal absent search modes.

Description of a Preferred Embodiment

Referring to FIG. 2, a selective call receiver (such as a pager) is powered by battery 20 which may be a AAA sized battery. The battery supplies operating power for the circuits within the selective call receiver. An antenna 21 receives POCSAG signal frequency modulated onto a radio signal. A receiver 22 receives the frequency modulated signal and through a process well known in the art demodulates and recovers the binary POCSAG signal which is output on the line 24. In the absence of POCSAG signals, the received signal on the line 24 has the equivalent of noise signals or other signals.

The received signal is processed by a decoder means 30, which includes functions shown enclosed by a broken line. The decoder means is driven by a clock 32, which may include a crystal, that provides a time base for decoding operations and the selection of one of two search modes described hereinafter. The received signal 24 is processed by a signal detector 38 which detects the presence or absence of the POCSAG baud rate, and a bit synchronizer 40 which bit synchronizes to the POCSAG signal. A bit clock signal 42 is used by a frame synchronizer 44 in order to detect the POCSAG sync code occurring within the received signal 24 and generate a framing signal 46 in response to detection of the sync code. In one embodiment, the bit synchronizer 40 may be a phase lock loop which is used to generate the bit clock, or in another embodiment the bit clock may be generated as a result of processes performed by the signal detector. An address decoder 48 uses the bit clock signal 42, and the framing signal 46 in order to detect a predetermined address occurring with the received signal 24. The address decoder 48 generates an alert signal 50 in response to the detection of the address. The alert signal 50 causes alert generator 52 to generate an alert which may be seen or heard by the user of the selective call receiver. A battery saver 54 periodically renders the receiver 22 operational. A controller 56 supplies timing signals to the functions within the decoding means 30 in order to cause the proper operation and cooperation of the functions in order to decode the POCSAG signal and to conserve power consumption. The controller 56 also reads a code plug 60 which includes information such as the predetermined address used by address decoder 48 and operational characteristics used by signal detector 38 and/or bit synchronizer 40. The signal detector 38 also selectively detects the absence of the desired POCSAG signal (noise, including other

unwanted signals) and produces an absence signal which is used by the controller 56 to cause the battery saver 54 to conserve power.

The functions of the control means 30 may be implemented in hardware circuits; however, the preferred embodiment implements these function blocks in a program having software routines which operate within host microcomputer. A host microcomputer such as the Motorola MC146805H2 microcomputer may readily implement these functions and is a preferred host microcomputer. Descriptions are well known in the art that enabling one skilled in the art to, with a microcomputer within a receiver, control the receiver, decode transmitted signal, and make the invention as described herein. Such descriptions include US Patent 4,518,961, US Patent 4,649,583, and US Patent 4,755,816 which are hereby incorporated by reference.

Figure 3 shows a block diagram of the signal detector 38 and the bit synchronizer 40 which operates in accordance with the present invention. A clock signal 100 having a frequency four times the desired baud rate, is derived from the clock 32, and provides timing for the operation of the signal detector 38 and bit synchronizer 40. The clock signal 100 drives phase generating means 102 which produces four phase signals 104 - 107. Each phase is independent and represents one half of a bit and each phase is spaced a quarter bit from the prior phase. This may be accomplished using a two bit counter 110 to drive a four phase generator 112.

The clock signal 100 also drives transition detecting means 115 which produces a transition signal 117 in response to a zero to one transition or a one to zero transition on the received signal input 24. A flip flop 119 is a "D" flip flop which samples and latches the data. An exclusive OR gate 121 compares the received signal 24 with the delayed signal from the flip flop 119. If a transition has occurred, the exclusive OR gate 121 will produce a pulse in response to the transition. The pulse is latched by a flip flop 123, the output of which produces the transition signal 117.

A counting means 130 operates during an integration time and has nine accumulators 131-139 or counting registers. Accumulators 131-134 and 135-138 are selectively enabled by the four phase signals 104-107 respectively, each accumulator being enabled for one half of a bit time. Accumulators 135-139 may be referred to hereinafter as image registers 135-138. If a transition signal occurs while an accumulator is enabled, the accumulator is decremented. The accumulator 139 is always enabled during the integration time and is decremented in response to each

transition signal. The values within accumulators 131-135 represent transitions accumulated during each of four one half bit intervals. Image registers 135-138 operate similarly to corresponding accumulators 131-134 with the exception that the image registers 135-138 are either incremented or decremented in response to a signal from a divider 140. The signal causes an image register to increment in response to an edge occurring on even bits and to decrement in response to a edge occurring on odd bits (even and odd being arbitrarily assigned).

In operation, for example, a controller 145 determines to search for the presence of a signal (i.e., a first search mode) having a predetermined baud rate and reads initialization values from the code plug 60. The counting means 130 is programmed to search for the presence of a signal by initializing each accumulator 131-134 with a value of 13, clearing image registers 135-138 and initializing the total accumulator 139 with a value of 16 and sampling the received signal. If any accumulator 131-134 reaches a value of zero before the total accumulator 139 reaches a value of zero, a signal is detected. If however, the total accumulator 139 reaches a value of zero first, the absence of signal is detected. Upon detection, the absolute value of image registers 135-138 is examined. If every register has a value less than or equal to 12, the presence of the desired baud rate is determined.

In another example of operation, the counting means 130 may be programmed to search for the absence of a signal (i.e., a second search mode) having a predetermined baud rate by initializing each accumulator 131-134 with a value of 4, clearing image registers 135-138 and initializing the total accumulator with a value of 16 and sampling the received signal. If every accumulator 131-134 reaches a value of zero before the total accumulator 139 reaches a value of zero, a signal absence is detected. If however total accumulator 139 reaches a value of zero first, signal is detected. Upon detection of the presence of signal, the absolute value of image registers 135-138 is examined. If every register has a value less than or equal to 12, the presence of the desired baud rate is determined.

In either of the first or second search modes, a bit clock indicative of the center of the bit may be established in response to the detection of the predetermined baud rate and the values within accumulators 131-134. Also the controller 145 initializes a timer 148 in response to values in the code plug 60. If the timer 148 times out before either signal or absence of

signal is detected, the received signal has too few transitions, and the absence of signal is determined.

An analyzing means 150, monitors accumulators 131-134 and 139, and the timer 148 in order to determine the presence or absence of signal. Additionally, the analyzing means 150 generates a signal 155 which selects one of eight phases for center sampling the bits within the signal upon detecting the presence of the baud rate. The operation of the analyzing means 150 is described in more detail with respect to Figures 5 and 6.

In response to signal 155, a bit clock generating means 168 generates a bit clock 42 on one of eight phases. The bit clock generating means 168 has an eight phase generator 162 which is responsive to the clock signal 100 and the two bit counter 102. The combination provides for the selection of four phases equivalent to the four phases which drive the counting means as well as four more phase in between. One of the outputs of a phase generator 162 is selected by a selector 164 in response to the signal 155, thereby establishing the bit clock.

In acccordance with the preferred embodiment, the controller 56 selects one of the first and second search modes by comparing the time of day with a predetermined time of day in a manner described hereinafter.

While Figure 3 shows a hardware implementation of the invention, Figures 4, 5 and 6 show a software implementation of the invention operating within a microcomputer. Figure 4 shows signal detection and bit synchronization as a task operating in a multi-tasking program operating within the microcomputer operating within the selective call receiver. Step 200 is indicative of the signal processor operations such as battery saving, frame synchronization, addresses detecting and message decoding. Step 202 determines if it is time to perform a signal search. If false, the program returns to step 200. If true, step 204 determines if the controller 56 selected either the signal presence search mode or search for the signal absence search mode. If the signal presence search mode is selected, step 206 reads the maximum integration time from the code plug and step 208 reads the absence threshold and total edge count from the code plug corresponding to the signal presence search mode. Then in step 210 the signal search routine is executed. The signal search routine is described in Figures 6 and 7. Alternately, if in step 204, the signal absence mode is selected, step 212 reads the maximum integration time from the code plug and step 214 reads the signal threshold and total edge count from the code plug corresponding to the signal absence search mode.

Then the in step 210 the signal search routine is executed. Upon returning from the signal search routine, step 216 checks if signal was found. If false, the flowchart returns to step 200 wherein the signal processor responds to the absence of signal. If true, step 218 determines if the absolute value of any image register is greater than a threshold value contained in the code plug. If false, the desired baud rate is detected and step 220 enables the bit clock with the selected phase from the signal search routine. The program then returns to step 200 for continued signal processing. If in step 218 an image accumulator is equal to or greater than the threshold, step 222 checks if the threshold has been executed after three consecutive executions of step 210. If false, the program returns to step 210 to again attempt signal searching, after which steps 216 or 218 can cause the program to return to step 200. If however step 220 is executed three consecutive times, the presence of a signal having a baud rate being an integer divisor is determined, and the program returns to step 200 wherein the signal processor responds to the absence of a signal being detected. It should be appreciated that the value of "three" in step 222 may be any positive non-zero integer value and may be stored in the code plug. Furthermore, in alternate embodiments, execution of step 222 may further initialize the signal search routine to values different from the values selected by either steps 206-208 or 212-214.

The flowchart of Figure 5 shows the operation of the signal search routine 210 of Figure 4. The flowchart is entered at step 240 where the four accumulators 131-134, the total accumulator 139, and the time 148 are initialized to values selected by the flow chart of Figure 4. Additionally, values X, Y, and image accumulators are initialized to "0", and the received signal is initially sampled.

Then step 242 adds 1 to X and if X=5 then changes X=1. This has the overall effect of producing X equal to values 1 through 4 and then return to 1. Step 242 further adds 1 to Y and if Y=9 then changes Y=1. This has the overall effect of producing Y equal to values 1 through 8 and then return to 1. Step 242 additionally decrements the time value, delays one quarter of a bit and samples the received signal. Step 244 then checks if the time value = 0. If true, there are too few transitions in the received signal to determine the presence of the predetermined baud rate and step 250 returns to the calling routine to indicate the absence of the signal. Otherwise, step 252 checks if an edge is detected by comparing the latest sample of the received signal with an immediately prior sample. If the

same, an edge is not detected and the flowchart returns to step 242. If true, the edge is processed.

The value X indicates one of four sample windows used to sample the received signal. Each sample window has a corresponding and unique combination of accumulators within the multiplicity of accumulators 131-134. A transition in one of the four windows causes a count to be changed in the corresponding accumulators. Step 254 shows which two of the accumulators are decremented in response to an edge being detected in a sample window. Additionally, the total accumulator is decremented. Then the flowchart executes step 256 which shows how the image registers count in response to an edge detected in a sample window and the value of Y.

Step 258 checks if any accumulator 131-134 has a value less than or equal to zero. If false, step 260 checks if the total accumulator has a value of zero. If false, the flowchart returns to step 242. If true, it is determined that signal is not found and the flowchart proceeds to step 250 as previously described. Referring back to step 258, if any accumulator has a value zero less than or equal to, step 262 checks if the signal presence search mode is selected. If true, the conditions for the detection of the presence of signal have been met and step 270 proceeds to a routine of Figure 6 to respond to the presence of the signal. If the signal presence search mode has not been selected, step 262 proceeds to step 272 to check if every accumulator 131-134 has a value of zero. If true, the conditions for the absence of signal have been met and the aforementioned step 250 is executed. If false, step 274 checks if the total accumulator equals zero. If true, the conditions for the presence of signal have been met and the aforementioned step 270 is executed. If false, the flowchart returns to step 242 to continue processing information.

Figure 6 shows selecting the phase of the bit clock in response to the detection of the presence of the signal. The determination of the presence of the signal has been indicated by execution of step 270 of Figure 5. Step 280 creates a four bit vector in response to the values within the four accumulators 131-134. Effectively, a zero is generated for each accumulator if the accumulator has a value of zero or less, otherwise a one is generated for the accumulator. Step 282 then determines the appropriate phase for the sample clock in response to the vector. Observe that the same table applies to either the selection of the signal presence search mode or the signal absence search mode. In response to the vector, one of eight phases

is selected corresponding to phases A-H. The phase selection corresponds to the generation of signal 155.

Figure 7 illustrates the response of the signal detector to a strong signal. Line 300 corresponds to eye patterns of a received signal under strong signal conditions, wherein transitions occur at events 302, 304 and 306. Line 310 shows the occurrence of sample windows 1-4 with respect to transitions 302-306. The transitions all occur within sample window 2. Each time a transition occurs in sample window 2, accumulators 1-2 and 2-3 are decremented. Under strong signal, transitions of this example will always occur in window 2.

If the signal presence search mode was selected (i.e., peak time); accumulators 131-134 were initialized with 13; the total was initialized with 16; and all of the transitions occurred within sample window 2, after the occurrence of 13 transitions, accumulators 1-2 and 2-3 would simultaneously reach a value of zero, thereby satisfying the signal found criterion. The resulting 4 bit vector would be 0011 which according to the table of step 282, results in the selection of phase "H". Line 315 shows the occurrence of sample signal 42 with respect to bits defined by transitions 302-306. The selection of phase "H" on line 315 substantially corresponds to the center of each bit.

Alternately if: the signal absence search mode was selected (i.e., off peak time); accumulators 131-134 were initialized with 4; the total was initialized with 16; and all of the transitions occurred within sample window 2, only accumulators 1-2 and 2-3 would decrement while accumulators 3-4 and 4-1 would remain at their initialized value. After 16 transitions, the total accumulator would equal zero, thereby satisfying the signal found criterion. The resulting 4 bit vector would again be 0011 which according to the table of step 282, again results in the selection of phase "H".

Thus in the example of the signal of Figure 7, if the signal presence search mode were selected, the signal would be detected after 13 transitions, while in the signal absence search mode were selected, the presence of the signal would be detected after 16 transitions. Thus, by anticipating the presence of the signal, the signal may be more rapidly detected. Searching in the desired signal search mode instead of the signal absence mode during the times of day when most transmissions occur would most likely save battery power. Conversely, searching in the signal

absence mode instead of the signal search mode during the times of day when few transmissions occur would save battery power.

Figure 8 illustrates the response of the signal detector to a weak signal. Line 320 corresponds to eye patterns of a received signal under weak signal conditions, wherein transitions occur at events 322, 324 and 326. Under weak signal conditions, the location of transitions are randomly affected by noise. Line 330 shows the occurrence of sample windows 1-4 with respect to transitions 322-326. Transitions 322 and 326 occur within sample window 1 while transition 324 occurs within sample window 2. Each time a transition occurs in sample window 1, accumulators 4-1 and 1-2 are decremented. Each time a transition occurs in sample window 2, accumulators 1-2 and 2-3 are decremented. Under weak signal, transitions of this example will occur in either windows 1 or 2.

If the signal search presence mode was selected (i.e., peak time); accumulators 131-134 were initialized with 13; the total was initialized with 16; and all of the transitions occurred within sample windows 1 and 2, after the occurrence 13 transitions, accumulator 1-2 would reach a value of zero since it is decremented in response to transitions detected in either window 1 or 2. This satisfies the signal found criterion. The resulting 4 bit vector would be 0111 which according to the table of step 282, results in the selection of phase "G". Line 335 shows the occurrence of sample signal 42 with respect to bits defined by transitions 322-326. The selection of phase "G" on line 335 substantially corresponds to the center of each bit.

Alternately if the signal absence search mode was selected (i.e., off peak time) and accumulators 131-134 were initialized with 4, the total was initialized with 16, and all of the transitions occurred within sample windows 1 and 2, only accumulators 4-1, 1-2 and 2-3 would decrement while accumulators 3-4 would remain at it's initialized value. After 16 transitions, the total accumulator would equal zero, thereby satisfying the signal found criterion. The resulting 4 bit vector would be 0010 which according to the table of step 282, again results in the selection of phase "G".

Thus, as in the example of the signal of Figure 7, Figure 8 also shows that correctly anticipating the presence of signal results in more rapid signal detection. Furthermore, Figures 7 and 8 show selection of identical center sample phases from either the signal presence search mode or the signal absence search mode.

Figure 9 illustrates the response of the signal detector to the absence of a signal (i.e., off peak time), or the presence of noise. Line 340 corresponds to transition patterns of the received signal noise, wherein transitions occur at events 342-348. Line 350 shows the occurrence of sample windows 1-4 with respect to transitions 342-348. The transitions effectively occur randomly within sample windows 1-4 (although transitions are shown only occurring within windows 1, 2 and 4). Each time a transition occurs in a sample window, the corresponding accumulators are decremented. Under noise conditions, on the average, the same number of transitions will occur within every sample window.

If: the signal search mode was selected (i.e., peak time); accumulators 131-134 were initialized with 13; the total was initialized with 16; and the transitions randomly occurred within every window, after the occurrence 16 transitions, an average of 4 transitions would have occurred within each sample window causing each accumulator to be decremented by 8, leaving a remainder of 5 in each accumulator. Thus the criterion for signal has not been met within the 16 total transitions, thereby satisfying the signal absence criterion.

Alternately, if: the signal absence search mode was selected (i.e., off peak time); accumulators 131-134 were initialized with 4; the total was initialized with 16; and transitions occurred every third window, within 8 transitions all of the accumulators would decrement to zero, thereby satisfying the criterion for the absence of signal detection.

Thus, in the example of the signal of Figure 9, if the signal presence search mode were selected, the absence of signal would be detected after 16 transitions, while in the signal absence search mode, the absence of the signal would be detected after 8 transitions. Thus by correctly anticipating the absence of the signal, the absence of signal may be more rapidly detected. It should be appreciated that an optimum distribution of noise transitions has been selected for this example, and typically more transitions will be required to correctly detect noise.

Figure 10 illustrates the response of the signal detector to a strong signal having the desired baud rate. Line 360 corresponds to eye patters of a received signal under strong signal conditions, wherein transitions occur at events 362, 364 and 366. Line 370 shows the occurrence of sample windows 1-4 with respect to transitions 362-346. The transitions all occur within sample window 2. Each time a transition occurs in an even sample window 2, image registers 1-2 and 2-3 are decremented, and each time a

transition occurs in an odd sample window 2, image registers 1-2 and 2-3 are incremented. Under strong signal, transitions of this example will always occur in window 2.

If a transition occurs every bit interval the image registers will be decremented as many times as will be incremented. Independent of the selected signal search mode, if the total was initialized with 16, and signal was detected between 13 and 16 transitions, all of the image accumulators would have a value substantially equivalent to zero, thereby satisfying the signal found criterion.

Figure 11 illustrates the response of the signal detector to a strong signal having the baud rate one half of the desired baud rate. Line 380 corresponds to eye patters of a received signal under strong signal conditions, wherein transitions occur at events 382 and 386. Line 390 shows the occurrence of sample windows 1-4 with respect to transitions 382 and 386. The transitions all occur within an even sample window 2 in response to which image registers 1-2 and 2-3 are decremented, however, no transition occurs in an odd sample window 2, thus image registers 1-2 and 2-3 are not incremented. If a transition occurs every even bit interval the image registers will be only be decremented. Independent of the selected signal search mode, if the total was initialized with 16 and signal was detected between 13 and 16 transitions, image registers 1-2 and 1-3 would have absolute values greater than or equal to 13. If the threshold for any image register were determined to be 12, signal found criterion would not be met according to step 218 of Figure 4.

Thus the invention is capable of simultaneously detecting the presence of signal having a predetermined baud rate having transitions randomly occurring between bits while positively determining that the detected baud rate that is not an integer divisor of the predetermined baud rate.

Figure 12 shows a table indicating the operation of the invention under conditions similar to those of Figure 7. In the example, a total of 16 transitions are recorded. The first two rows show that 15 transitions occur in sample window 2 and one transition occurs in sample window 3. The third and forth rows show the counts accumulated in accumulators 131-134. In the signal presence search mode, the fifth row shows the resulting vector used in step 282 with a signal threshold of 13. In actuality the signal would have been determined to be found after any accumulator accumulated 13 counts. This vector assumes the transition that occurred

in window 3 occurred after the 13th transition. Had the transition occurred prior to the 13th transition, accumulator 2-3 would accumulate 13 counts before any other, resulting in a vector of 1011 which would result in a phase of "A" as opposed to a phase of "H" which results from the 0011 vector shown in the fifth row. The sixth row shows the resulting vector in the signal absence search mode.

Figure 13 shows a table indicating the operation of the invention under conditions similar to those of Figure 8. In the example, a total of 32 transitions are recorded. The first two rows show that 14, 12, 1 and 5 transitions occur in sample window 1, 2, 3 and 4 respectively. The third and fourth rows show the counts accumulated in accumulators 131-134. In the signal presence search mode, the fifth row shows the resulting vector used in step 282 with a signal threshold of 26. In actuality the signal would have been determined to be found after the total accumulator accumulated 26 counts, which may have occurred any time between the 26th and 32nd transition depending upon the received signal. The sixth row shows the resulting vector in the signal absence search mode.

Figure 14 shows a table indicating the operation of the invention under conditions similar to those of Figure 9. In the example, a total of 16 transitions are recorded. The first two rows show that 4, 6, 2 and 4 transitions occur in sample windows 1, 2, 3 and 4 respectively. The third and forth rows show the counts accumulated in accumulators 131-134. In the signal presence search mode, the fifth row shows the resulting vector which indicates that signal absence is detected. The sixth row shows the resulting vector in the signal absence search mode. As explained with respect to Figure 9, this vector could occur any time between the 8th and 16th transition.

In one application of the invention, three parameters may be adjusted to govern the performance of the invention.

The first parameter is the total edge count. By increasing this parameter, the ability of the invention to distinguish the signal from noise or other signals is improved. This is because the invention has more samples from which to make a judgement. This ability is improved at the expense of the extra power consumed in order to accumulate the additional transitions. For example if in the signal of Figure 13 only 16 samples were taken and a threshold of 13 was used, the presence of the signal may have been incorrectly missed depending upon the occurrence of the transitions, while the presence of the signal was found using 32

transitions. The first 16 transitions may have occurred 5, 6, 1, 4 in windows 1, 2, 3 and 4 respectively. On the other hand if the signal of Figure 13 was determined to be absent (by having selected a threshold of 28 instead of 26) and only 16 samples were taken and a threshold of 14 used, the presence of the signal may have incorrectly been detected. The first 16 transitions may have occurred 7, 7, 1, 1 in windows 1, 2, 3 and 4 respectively. Thus by taking more samples a more accurate determination may be made.

False detection of the presence of a signal is undesirable because in response to a signal detection, the selective call receiver maintains the operation of the receiver for a long interval thereafter in order to detect a POCSAG sync code. Since noise is present, no sync code will be found. Thus battery power is unnecessarily expended searching for sync code and the battery life of the selective call receiver degrades. However, different selective call receiver applications may require different sensitivity and falsing characteristics, the invention provides adjusting the sensitivity and falsing performance. Furthermore, with the advent of POCSAG 1200 baud protocol, the invention provides a means for rejecting GSC signals having 600 and 300 baud data rates, thereby eliminating a major source of falsing.

The second parameter is the threshold count, either in the signal present search mode or the signal absent search mode. This parameter establishes the relative sensitivity of the signal detection. For example Figure 13 shows a relatively noisy signal. If a signal threshold of 28 or a noise threshold of 5 where used, the invention would not have detected a signal. Adjusting the sensitivity allows the sensitivity of the invention to be matched to the desired system sensitivity or the individual selective call receiver sensitivity.

The third parameter is the maximum integration time. This parameter allows the invention to account for the maximum number of bits not having transitions. For example, if a signal having no transitions at all was received, it is desirable to determine the absence of the baud rate quickly in order to return to a power conservation mode. In practice, this parameter is chosen to substantially provide for the maximum time in which the total edge count may occur in the presence of the baud rate.

The loading for selective call receiver systems is highly dependent on the time of day because the primary users for selective call receiver systems are primarily active during conventional business hours. Other users require their selective call receivers to be active 24 hours a day and

these users account for most of the system loading during "off-hour" periods. The system loading for a typical selective call receiver system is graphically shown in FIG. 15. Early morning hours, 12:00 A.M. to 6:00 A.M. are usually lightly loaded times. As the day progresses, loading increases to reach "peaks" at approximately 8:00 A.M., 12:00 P. M., and 5:00 P.M. Since the likelyhood of a particular selective call receiver receiving a signal occurs during the peak hours, it would be most efficient to search for the signal in the signal present search mode during the peak hours. Conversely, the likelyhood of a particular selective call receiver receiving a signal is low during the off-peak hours, it would be most efficient to search for the signal in the signal absent search mode during the off-peak hours.

The selection of the signal present search mode or the signal absent search mode may be made in any of several methods. Two methods will be illustrated. First, referring to FIG. 16, the time of day is determined in step 400 by the controller 56 in response to the clock 32. If the time of day compares in step 402 with a predetermined time of day stored in the code plug, the select signal present search mode is selected. If the times do not compare in step 402, the signal absent search mode is selected, step 406. The predetermined times of day stored in the code plug may, for example, be programmed in the selective call receiver by the system user.

Referring to FIG. 17, a second method of selecting the signal present search mode or the signal absent search mode comprises perodically determining if a given time frame (i.e., a given time of day) is a peak time or an off-peak time. The time frame may be any period of time, e.g., a minute or an hour. At some point of time during that time frame, e.g., in the middle, the steps are initiated. If it is time to determine if the time frame is a peak transmission time, step 420, a determination is made if the selective call receiver is synchronous to the selective call receiver terminal, step 422. If yes, a shift register within the memory 60 is incremented with a "1", step 424, or if no, the shift register is incremented with a "0", step 426. If the shift register has a greater number of 1's, step 428, the signal present search mode is selected, step 430. However, if the shift register has a greater number of 0's, step 428, the signal absence search mode is selected, step 432. This shift register provides a dynamic window of history which allows the selective call receiver to examine the previous history on which it can make its own search mode determination without total dependency on a programmed time.

The invention provides a means for operating a microcomputer at a low bus rate. The invention samples the received signal at a relatively low rate of four times per bit, and only accumulates transitions in respective accumulators during the integration time. Only minor calculations and no phase adjustments are made during the integration time as in the prior art microcomputer based bit synchronizers. A simplified calculation is made on the distribution of the accumulations in order to detect signal or noise, that is to determine if one or all of the registers have a value of zero. As a result of the calculation, a bit clock in phase with the data can be established. The simplifications also reduce the demand for bus cycles, thus a means is provided which allows the microcomputer to operate at a lower bus rate during bit synchronization. This further reduces power consumption and extends the battery life of the selective call receiver. Additionally, the simple operation and reduced complexity of the invention provides implementation of the invention in integrated circuitry, without compromising the rapid detection aspects of the invention.

It can be appreciated that the invention in one form comprises only a signal presence or absence detector. In another form the invention comprises only a means for detecting the presence of a predetermined baud rate and the absence of a baud rate being an integer divisor of the predetermined baud rate.

Many modifications may be made to the invention while remaining within the spirit and scope of the invention. The invention although shown in conjunction with a POCSAG signal may be used in conjunction with other protocols having predetermined baud rate. Alternately, the accumulators may be analyzed any time after the conditions are met for the determination of the presence or absence of the signal. Additionally, more or less sample windows may be used. For example, if six sample windows were used, a transition occurring within a sample window may cause two or three accumulators to record the count, and analysis similar to the aforementioned analysis may be used to determine the presence or absence of the signal. It can further be appreciated that other embodiments may include a number of alterations. The phase setting of the bit clock is predetermined, in alternate embodiments, the number of possible phases of the bit clock can be increased and the bit clock's phase chosen by analyzing the values of the accumulators. For example, a weighted average of the accumulators can be used to determine the average location of the

transitions, and the bit clock can be set to be 180° out of phase with the average location. It should be further appreciated that the steps of selecting the phase of the bit clock can be disregarded, or the bit clock means 168 can be eliminated, and the invention can be used as a signal presence or absence detector. Furthermore, the invention has been described with respect to a binary signal having two levels per symbol. The invention may additionally operate on a signal having more than two levels per symbol wherein transitions occur between symbols. It should be further appreciated that in an alternate embodiment, the setting of synchronization parameters with the code plug can be eliminated.

CLAIMS

1. An apparatus comprising:

a receiver capable of receiving a plurality of signals, wherein more of the signals are received at a peak time than at an off peak time;

means for determining if the signals are being received by searching in a first search mode;

means for determining if the signals are not being received by searching in a second search mode; and

means for activating the first means during the peak time and activating the second means during the off peak time.

2. The apparatus according to claim 1 wherein the means for activating comprises means for comparing the current time with a predetermined time for defining the peak time and off peak time.

3. The apparatus according to claim 1 wherein the activating means comprises means for storing information regarding whether the receiver is synchronous to signals received during each of a pluality of time periods, wherein the peak time comprises the time periods when the receiver is mostly synchronous.

4. In a receiver capable of receiving a plurality of signals, wherein more of the signals are received at a peak time than at an off peak time, the method comprising the step of selecting a signal present search mode during the peak time and a signal absent search mode during the off peak time

5. The method according to claim 4 wherein the peak time is determined by the step of comparing the current time with a predetermined time.

6. The method according to claim 4 wherein the peak time is determined by the steps of:

determining whether the receiver is synchronous to signals received during each of a plurality of time periods;

storing information in response to an affirmative determination indicating a peak time for the respective time periods; and

storing information in response to a negative determination indicating an off peak time for the respective time periods.

7. An apparatus comprising:

a receiver capable of receiving a plurality of signals, each signal having transitions between first and second states occurring at a predetermined baud rate, wherein more of the signals are received at a peak time than at an off peak time;

means for determining if the signals are being received by searching for a signal having the predetermined baud rate;

means for determining if the signals are not being received by searching for noise; and

means for activating the first means during the peak time and activating the second means during the off peak time.

8. The apparatus according to claim 7 wherein the means for activating comprises means for comparing the current time with a predetermined time for defining the peak time and off peak time.

9. The apparatus according to claim 7 wherein the activating means comprises means for storing information regarding whether the receiver is synchronous to signals received during each of a pluality of time periods, wherein the peak time comprises the time periods when the receiver is mostly synchronous.

10. An apparatus for selectively detecting the presence or absence of a signal having transitions between symbols occurring at a predetermined baud rate, the means comprising:

a multiplicity of counting registers;

means for establishing an integer number of samples windows per symbol, each sample window having a corresponding unique combination of a plurality of counting registers within said multiplicity of counting registers;

means for selecting presence detection during a first time period and absence detection during a second time period;

means for receiving a signal potentially including the signal and producing a received signal having transitions;

means for sensing the transitions of the received signal occurring within each established sample window;

means for counting in the counting registers corresponding to each sample window in which a transition is sensed; and

means generating a presence signal in response to the selection of presence detection and a counting register having a first predetermined number of counts; and

means for generating an absence signal in response to the selection of absence detection and all of the counting registers exceeding a second predetermined number of counts.

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11. A method of selectively detecting the presence or absence of a signal having transitions between symbols occurring at a predetermined baud rate, the method comprising the steps of:

establishing an integer number of samples windows per symbol, each sample window having a corresponding unique combination of a plurality of counting registers within a multiplicity of counting registers;

selecting presence detection during at least a first time period and absence detection during at least a second time period;

receiving a signal potentially including the signal and producing a received signal having transitions;

sensing the transitions of the received signal occurring within each established sample window;

counting in the counting registers corresponding to each sample window in which a transition is sensed; and

generating a presence signal in response to the selection of presence detection and a counting register having a first predetermined number of counts; and

generating an absence signal in response to the selection of absence detection and all of the counting registers exceeding a second predetermined number of counts.

12. The method according to claim 11 wherein:

said step of generating the presence signal generates the presence signal in response to the counting register having the predetermined number of counts within the occurrence of a first predetermined number of edges; and

said step of generates generates the absence signal in response to all of the counting registers exceeding the second predetermined number of counts within the occurrence of a second predetermined number of edges.

13. The method according to claim 11 further comprising the steps of:

generating the absence signal in response to the selection of presence detection and any counting register not having the predetermined number of counts within the occurrence of a first predetermined number of edges;

generating a presence signal in response to the selection of absence detection and any of the counting register not exceeding the predetermined number of counts within the occurrence of a second predetermined number of edges.

14. The method according to claim 13 further comprising the step of generating a sample signal indicative of the center of the baud signal in response to the presence signal wherein the center is determined as a function of the values in the multiplicity of counting registers.

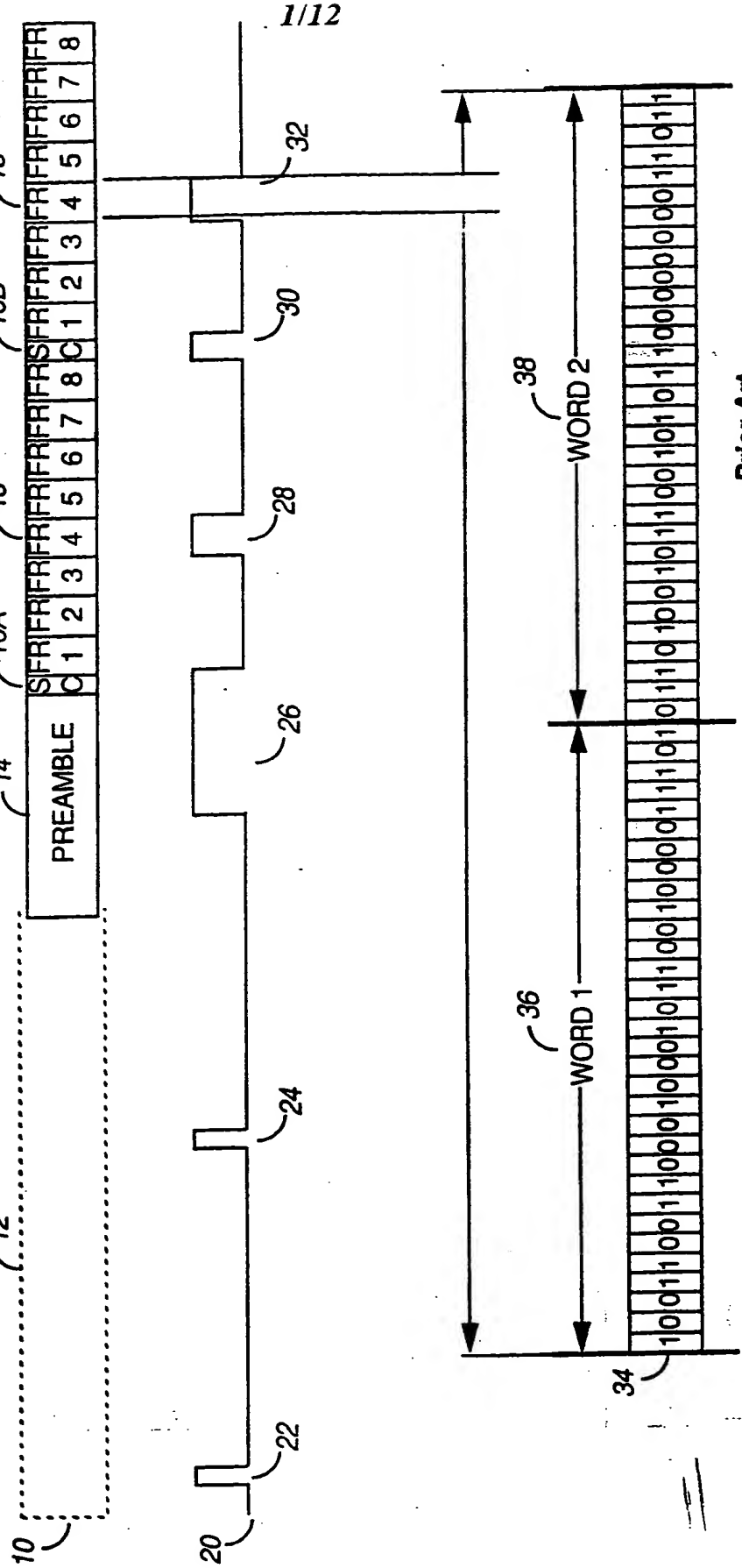
PREAMBLE
14
16A
16B
18
12
10
20
22
24
26
28
30
32
34
36
WORD 1
38
WORD 2
Prior Art

FIG. 1

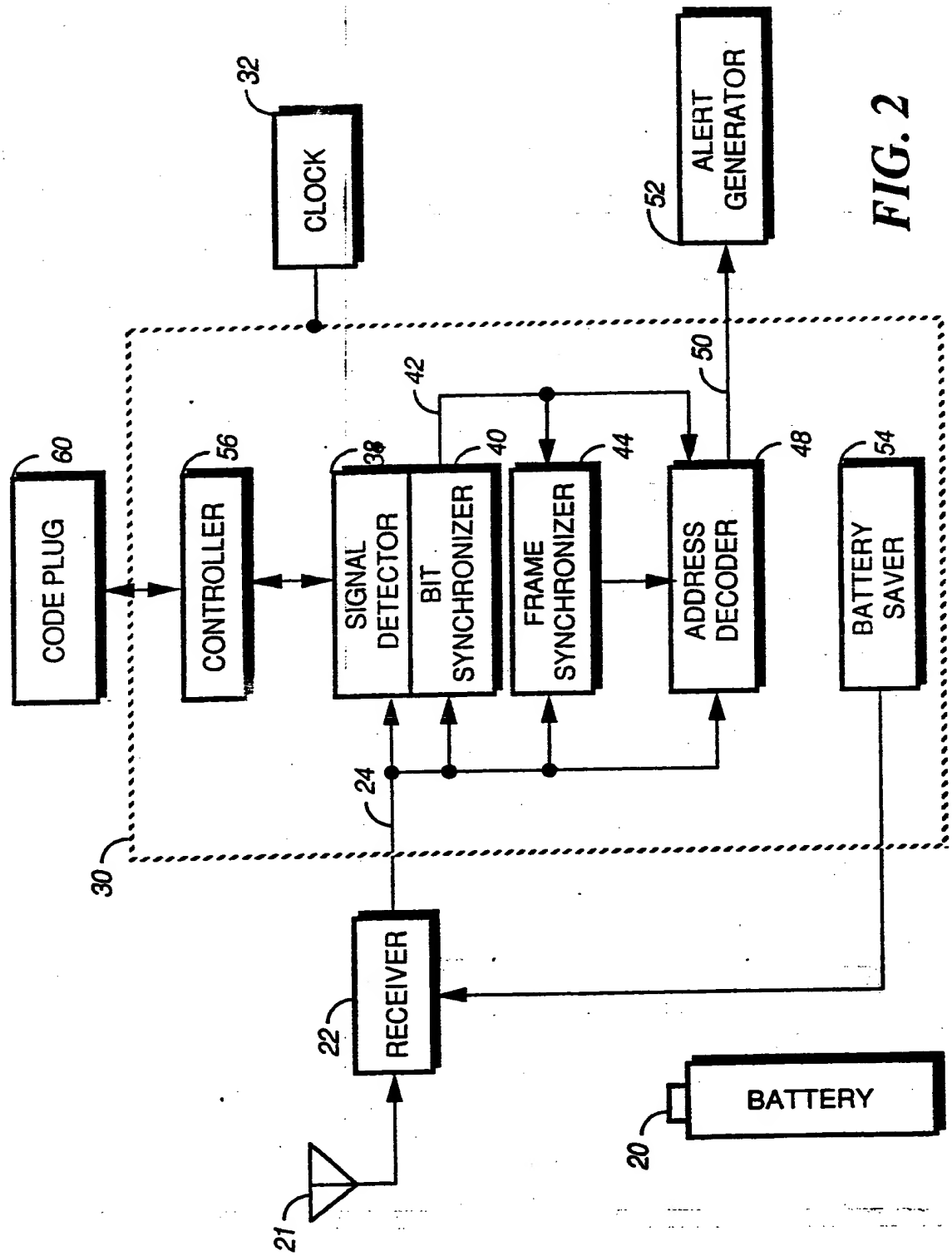
CLOCK
32
ALERT GENERATOR
52
50
42
CODE PLUG
60
CONTROLLER
56
SIGNAL DETECTOR
38
BIT SYNCHRONIZER
40
FRAME SYNCHRONIZER
44
ADDRESS DECODER
48
BATTERY SAVER
54
24
30
RECEIVER
22
BATTERY
20
21

FIG. 2

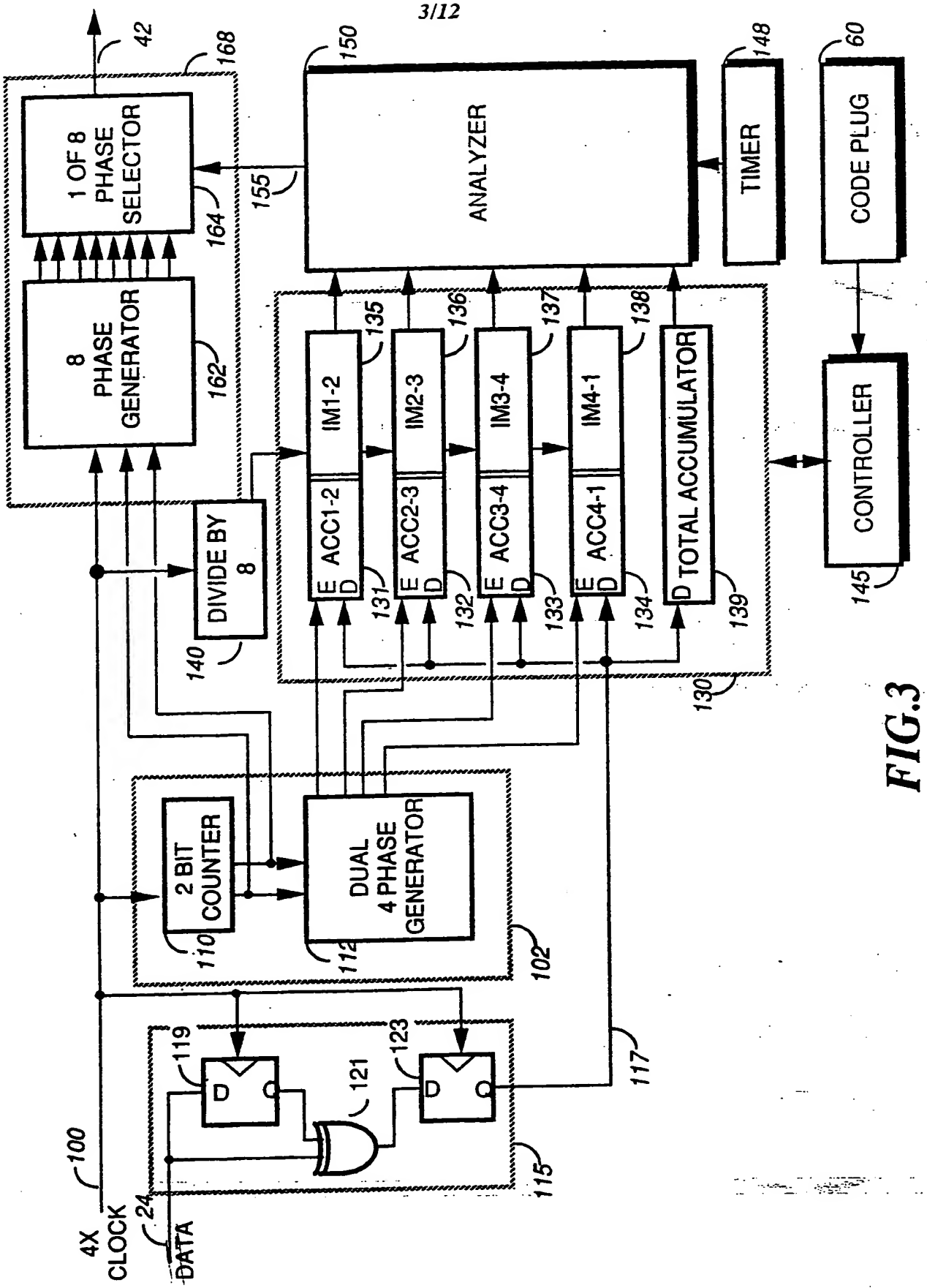
42
168
1 OF 8 PHASE SELECTOR
164
155
150
ANALYZER
148
TIMER
60
CODE PLUG
8 PHASE GENERATOR
162
IM1-2
135
IM2-3
136
IM3-4
137
IM4-1
138
TOTAL ACCUMULATOR
CONTROLLER
145
DIVIDE BY 8
140
ACC1-2
131
ACC2-3
132
ACC3-4
133
ACC4-1
134
139
130
2 BIT COUNTER
110
DUAL 4 PHASE GENERATOR
112
102
119
121
123
117
115
100
4X CLOCK
24
DATA

FIG.3

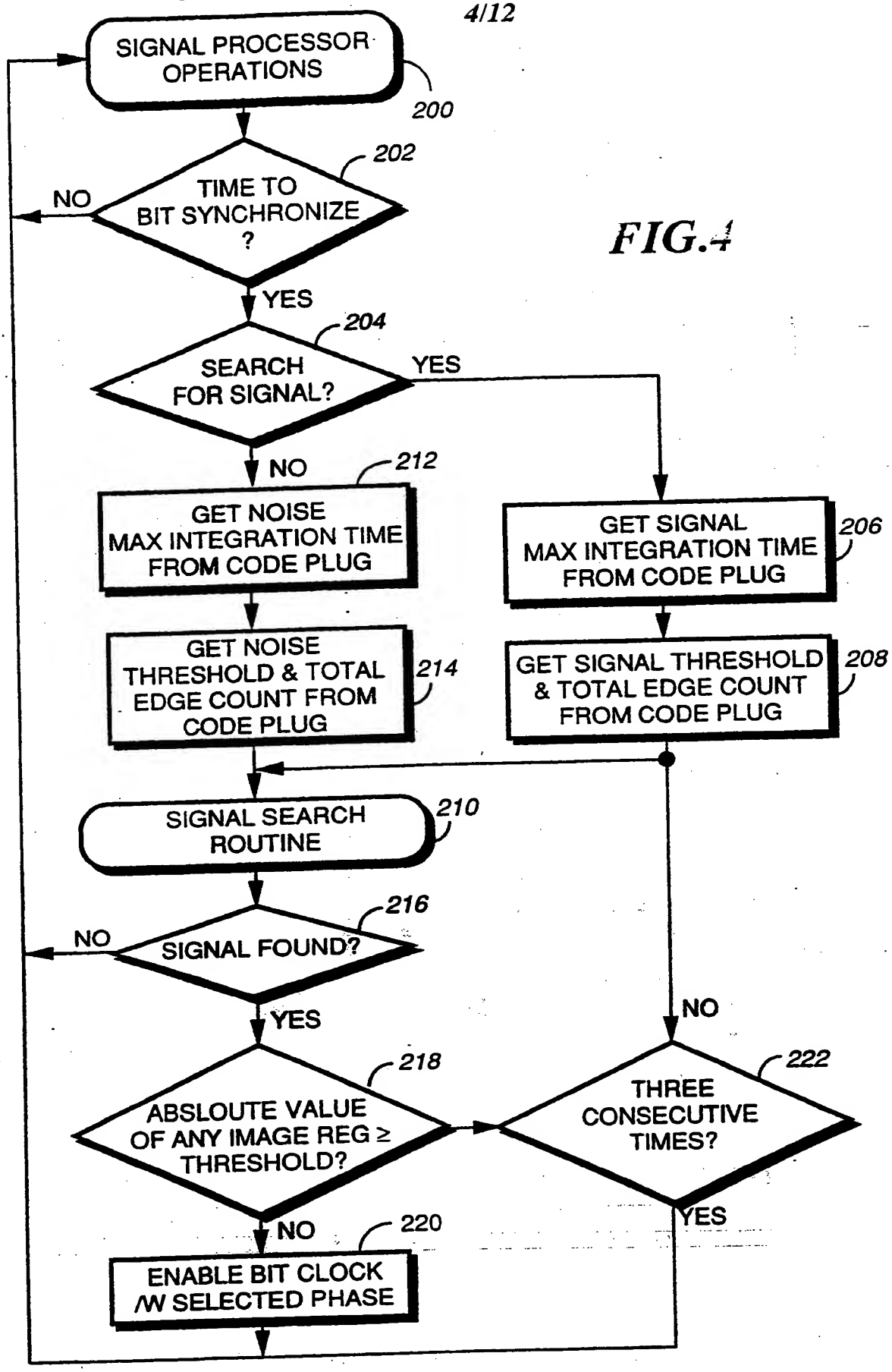
SIGNAL PROCESSOR OPERATIONS
200
202
TIME TO BIT SYNCHRONIZE ?
NO
YES
204
SEARCH FOR SIGNAL?
YES
NO
212
GET NOISE MAX INTEGRATION TIME FROM CODE PLUG
GET SIGNAL MAX INTEGRATION TIME FROM CODE PLUG
206
GET NOISE THRESHOLD & TOTAL EDGE COUNT FROM CODE PLUG
214
GET SIGNAL THRESHOLD & TOTAL EDGE COUNT FROM CODE PLUG
208
SIGNAL SEARCH ROUTINE
210
216
NO
SIGNAL FOUND?
YES
NO
218
ABSLOUTE VALUE OF ANY IMAGE REG ≥ THRESHOLD?
222
THREE CONSECUTIVE TIMES?
NO
YES
220
ENABLE BIT CLOCK /W SELECTED PHASE

FIG.4

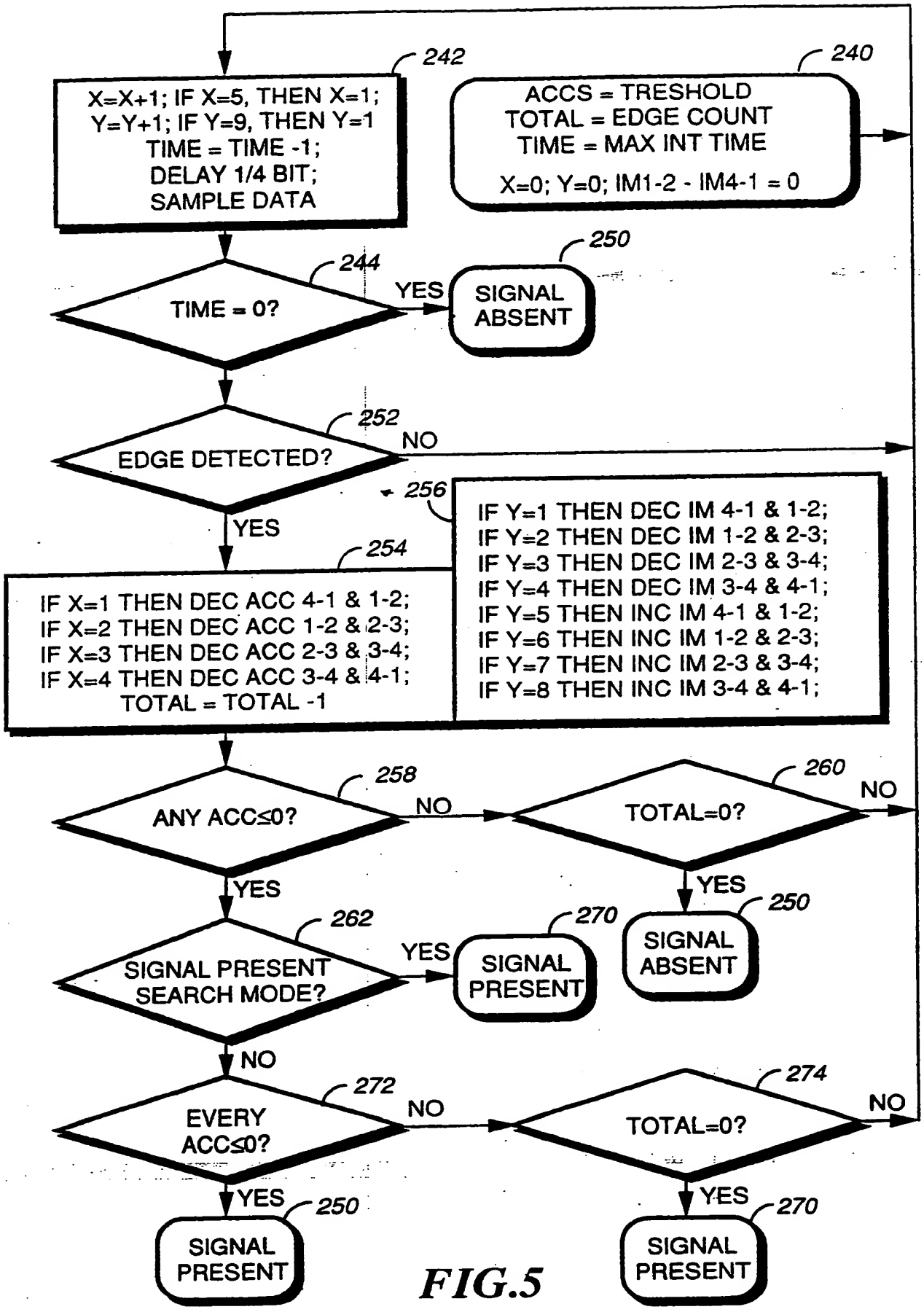
240
ACCS = TRESHOLD
TOTAL = EDGE COUNT
TIME = MAX INT TIME
X=0; Y=0; IM1-2 - IM4-1 = 0
242
X=X+1; IF X=5, THEN X=1;
Y=Y+1; IF Y=9, THEN Y=1
TIME = TIME -1;
DELAY 1/4 BIT;
SAMPLE DATA
244
TIME = 0?
YES
250
SIGNAL ABSENT
252
EDGE DETECTED?
NO
YES
256
IF Y=1 THEN DEC IM 4-1 & 1-2;
IF Y=2 THEN DEC IM 1-2 & 2-3;
IF Y=3 THEN DEC IM 2-3 & 3-4;
IF Y=4 THEN DEC IM 3-4 & 4-1;
IF Y=5 THEN INC IM 4-1 & 1-2;
IF Y=6 THEN INC IM 1-2 & 2-3;
IF Y=7 THEN INC IM 2-3 & 3-4;
IF Y=8 THEN INC IM 3-4 & 4-1;
254
IF X=1 THEN DEC ACC 4-1 & 1-2;
IF X=2 THEN DEC ACC 1-2 & 2-3;
IF X=3 THEN DEC ACC 2-3 & 3-4;
IF X=4 THEN DEC ACC 3-4 & 4-1;
TOTAL = TOTAL -1
258
ANY ACC≤0?
NO
260
TOTAL=0?
NO
YES
YES
262
SIGNAL PRESENT SEARCH MODE?
YES
270
SIGNAL PRESENT
250
SIGNAL ABSENT
NO
272
EVERY ACC≤0?
NO
274
TOTAL=0?
NO
YES
YES
250
SIGNAL PRESENT
270
SIGNAL PRESENT

FIG.5

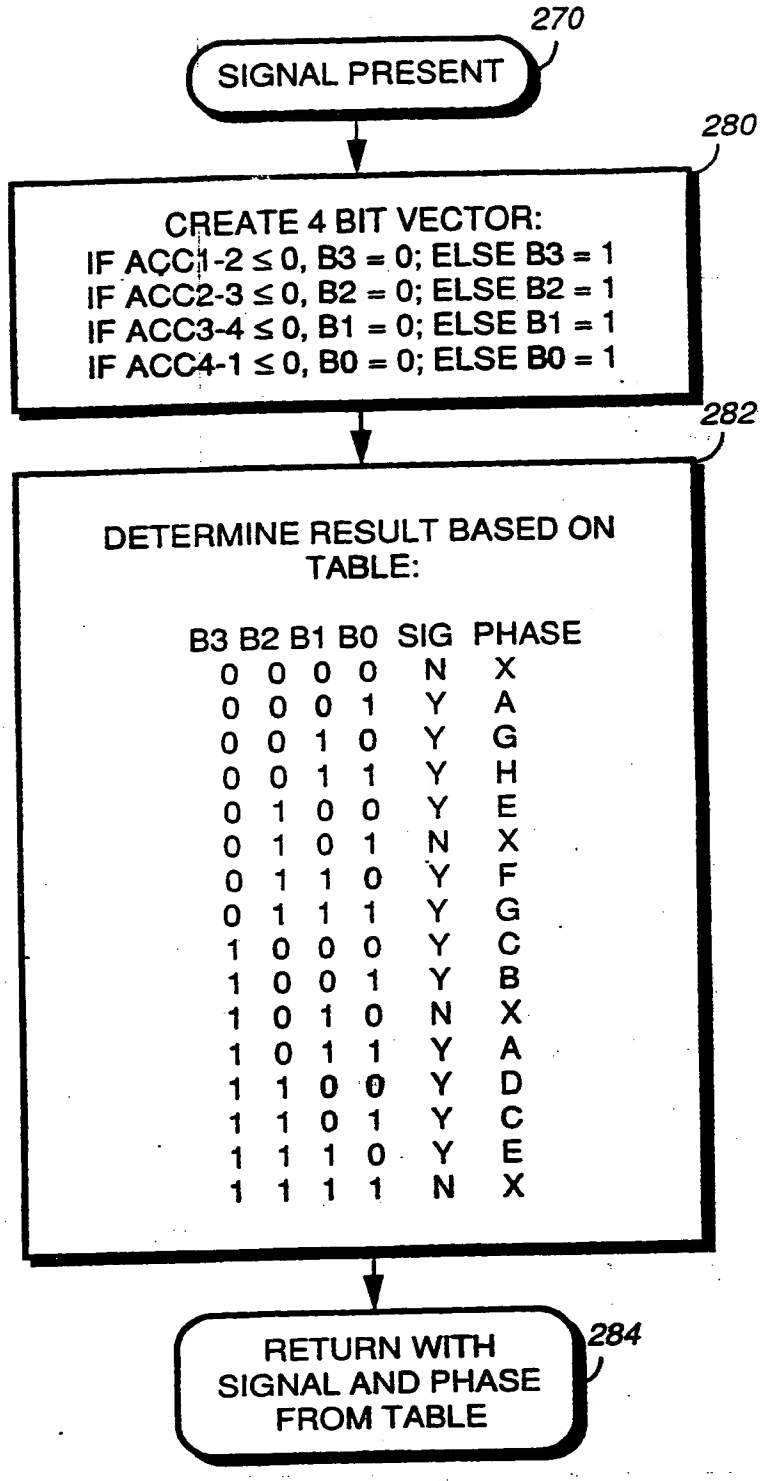
270
SIGNAL PRESENT
280
CREATE 4 BIT VECTOR:
IF ACC1-2 ≤ 0, B3 = 0; ELSE B3 = 1
IF ACC2-3 ≤ 0, B2 = 0; ELSE B2 = 1
IF ACC3-4 ≤ 0, B1 = 0; ELSE B1 = 1
IF ACC4-1 ≤ 0, B0 = 0; ELSE B0 = 1
282
DETERMINE RESULT BASED ON TABLE:
B3 B2 B1 B0 SIG PHASE
0 0 0 0 N X
0 0 0 1 Y A
0 0 1 0 Y G
0 0 1 1 Y H
0 1 0 0 Y E
0 1 0 1 N X
0 1 1 0 Y F
0 1 1 1 Y G
1 0 0 0 Y C
1 0 0 1 Y B
1 0 1 0 N X
1 0 1 1 Y A
1 1 0 0 Y D
1 1 0 1 Y C
1 1 1 0 Y E
1 1 1 1 N X
RETURN WITH SIGNAL AND PHASE FROM TABLE
284

FIG.6

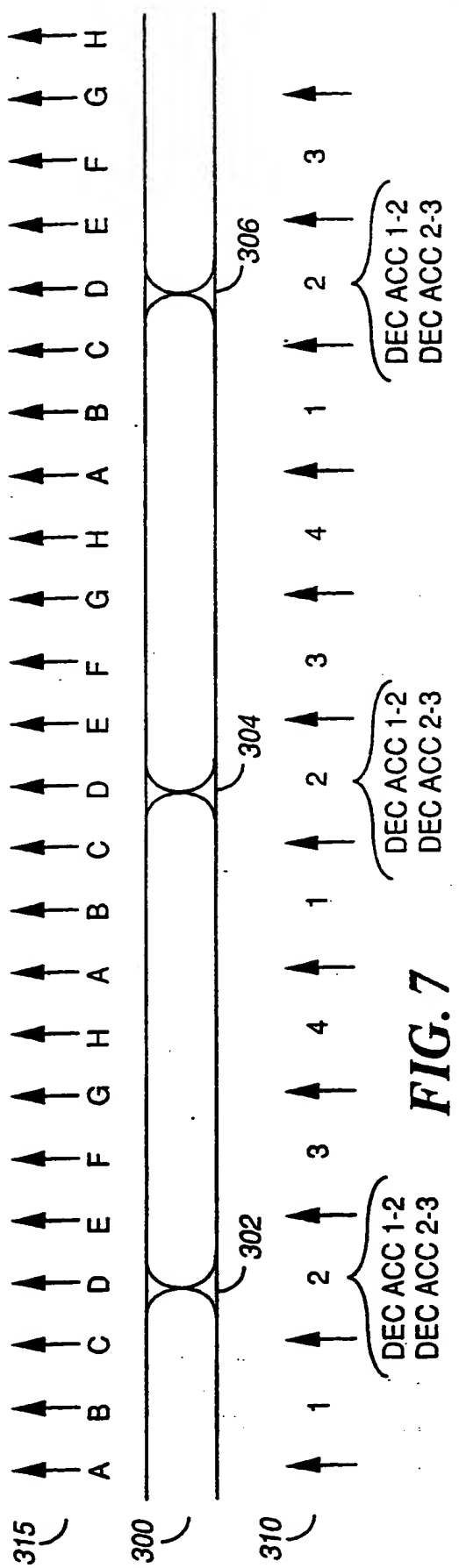

FIG. 7

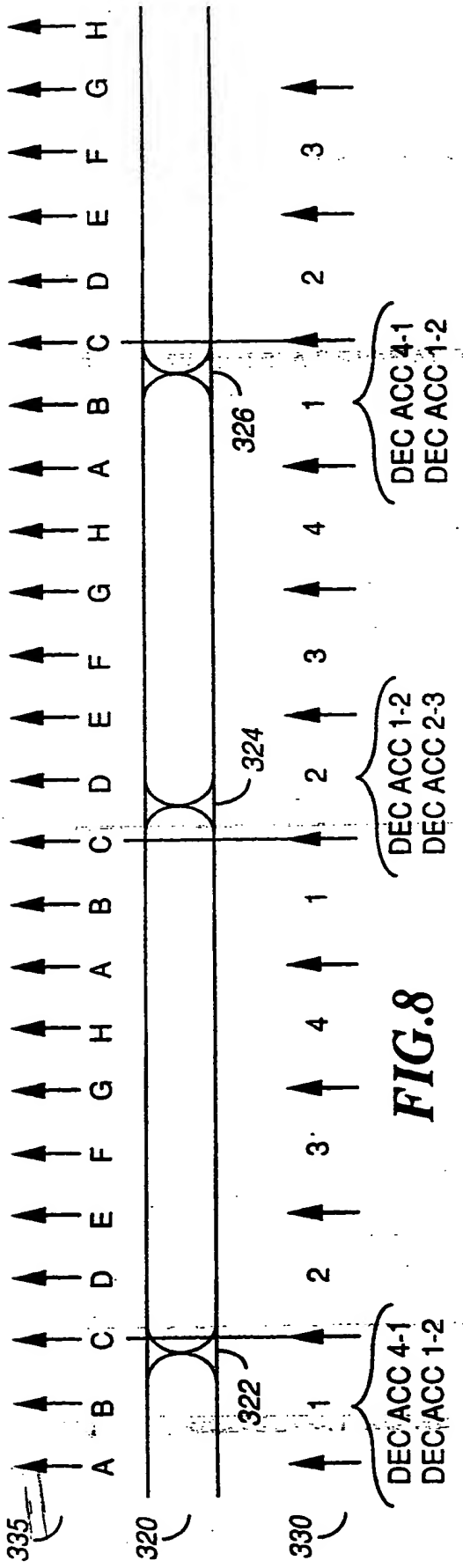

FIG.8

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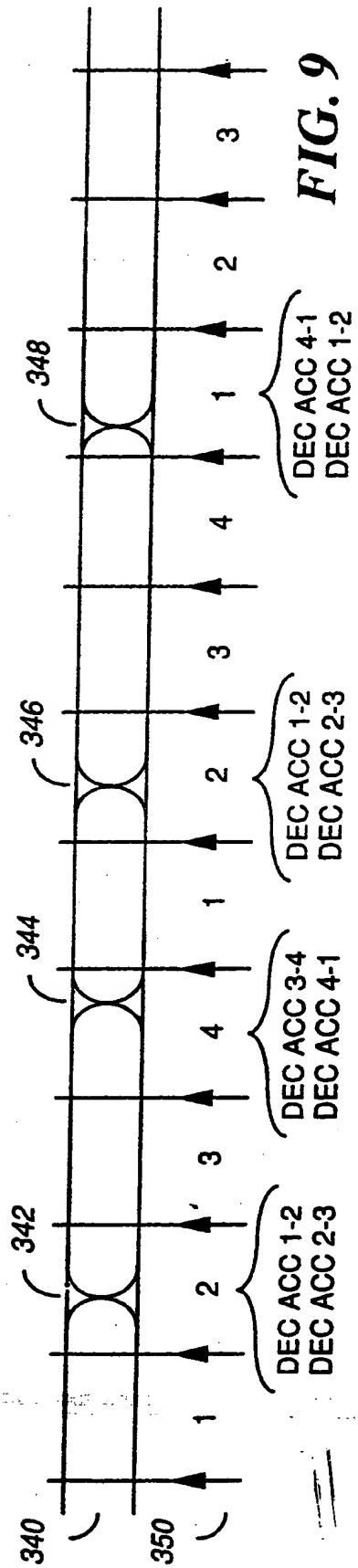

FIG. 9

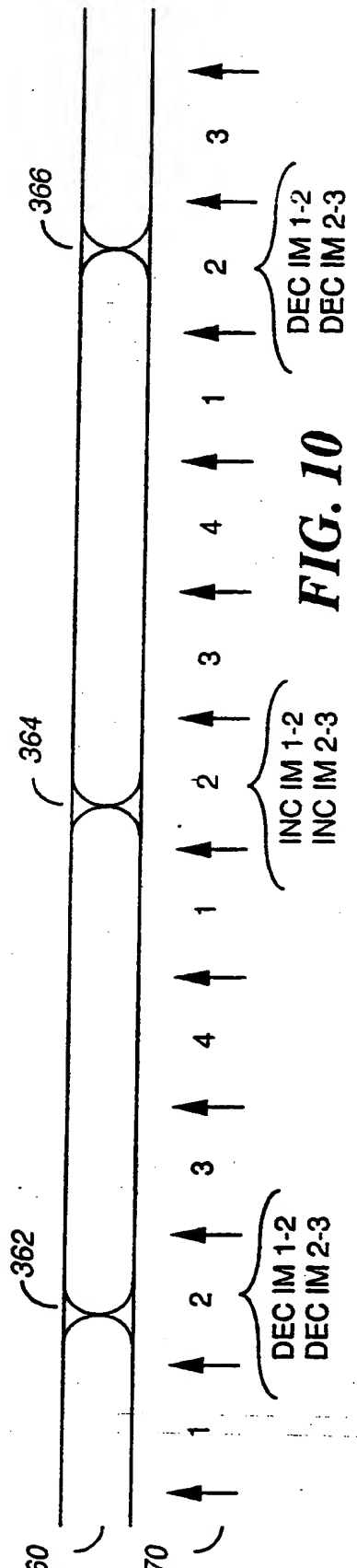

FIG. 10

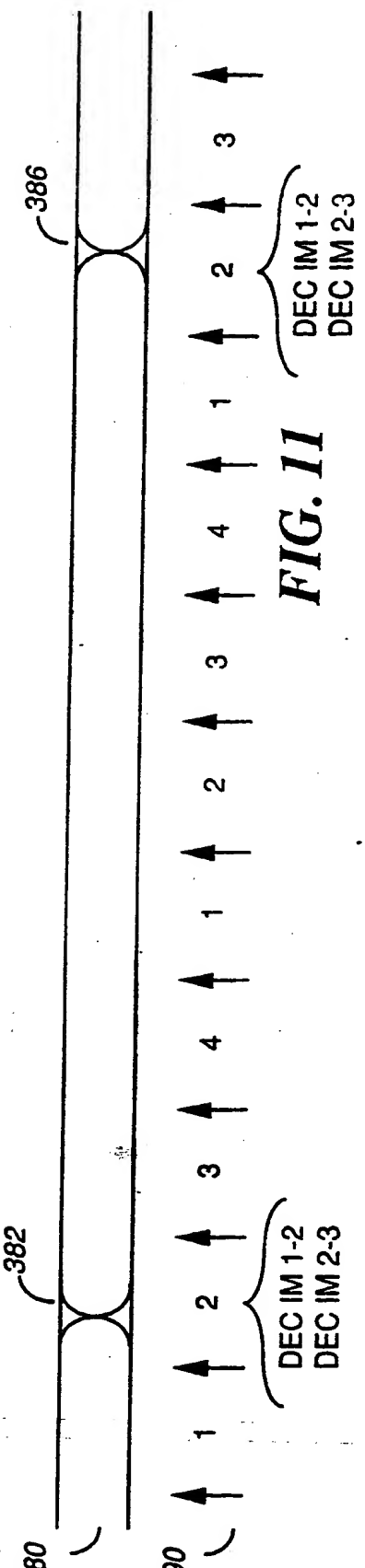

FIG. 11

SAMPLE WINDOW	1	2	3	4
TOTAL EDGES = 16	0	15	1	0
ACCUMULATED	1-2	2-3	3-4	4-1
COUNTS	15	16	2	0
RESULT AT SIGNAL THRESHOLD = 13	≤0	≤0	≥1	≥1
RESULT AT NOISE THRESHOLD = 4	≤0	≤0	≥1	≥1

FIG. 12

SAMPLE WINDOW	1	2	3	4
TOTAL EDGES = 32	14	12	1	5
ACCUMULATED	1-2	2-3	3-4	4-1
COUNTS	26	13	6	19
RESULT AT SIGNAL THRESHOLD = 26	≤0	≥1	≥1	≥1
RESULT AT NOISE THRESHOLD = 7	≤0	≤0	≥1	≤0

FIG. 13

SAMPLE WINDOW	1	2	3	4
TOTAL EDGES = 16	4	6	2	4
ACCUMULATED	1-2	2-3	3-4	4-1
COUNTS	10	8	6	8
RESULT AT SIGNAL THRESHOLD = 16	≥1	≥1	≥1	≥1
RESULT AT NOISE THRESHOLD = 4	≤0	≤0	≤0	≤0

FIG. 14

BNSDOCID: <WO 9119358A1>

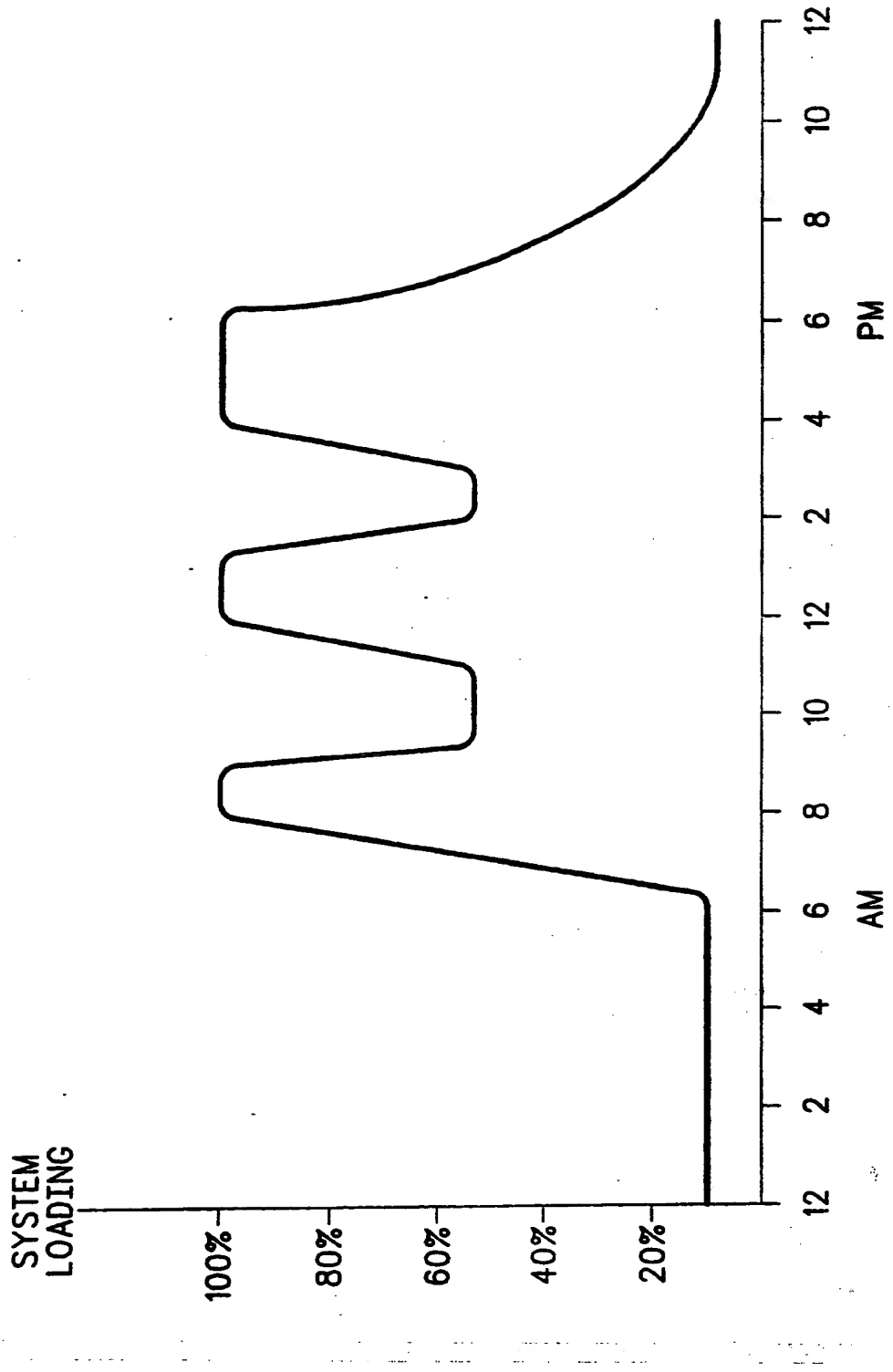
SYSTEM LOADING
100%
80%
60%
40%
20%
12
2
4
6
8
10
12
2
4
6
8
10
12
AM
PM
TIME OF DAY

FIG.15

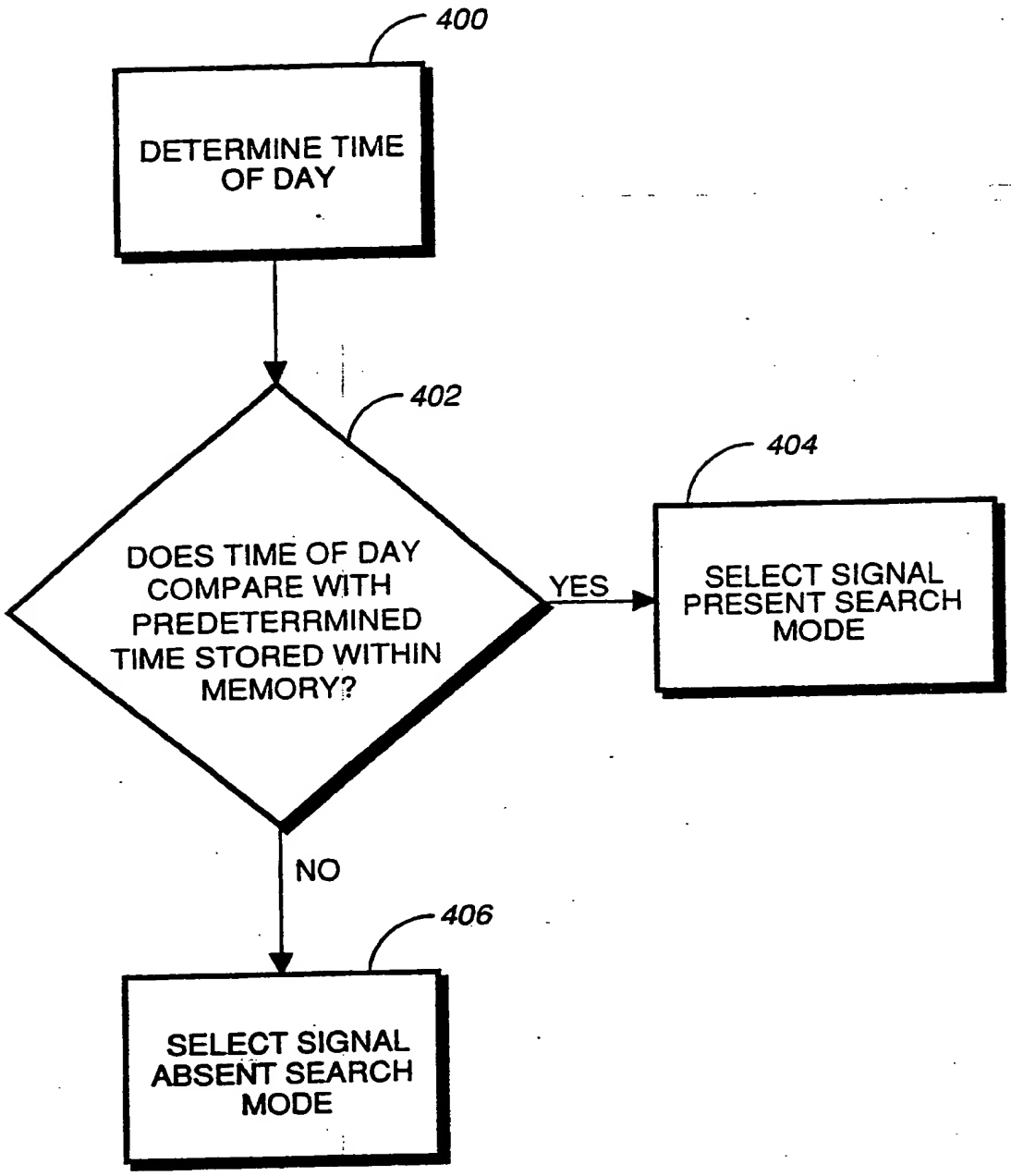
400
DETERMINE TIME OF DAY
402
DOES TIME OF DAY COMPARE WITH PREDETERRMINED TIME STORED WITHIN MEMORY?
YES
404
SELECT SIGNAL PRESENT SEARCH MODE
NO
406
SELECT SIGNAL ABSENT SEARCH MODE

FIG. 16

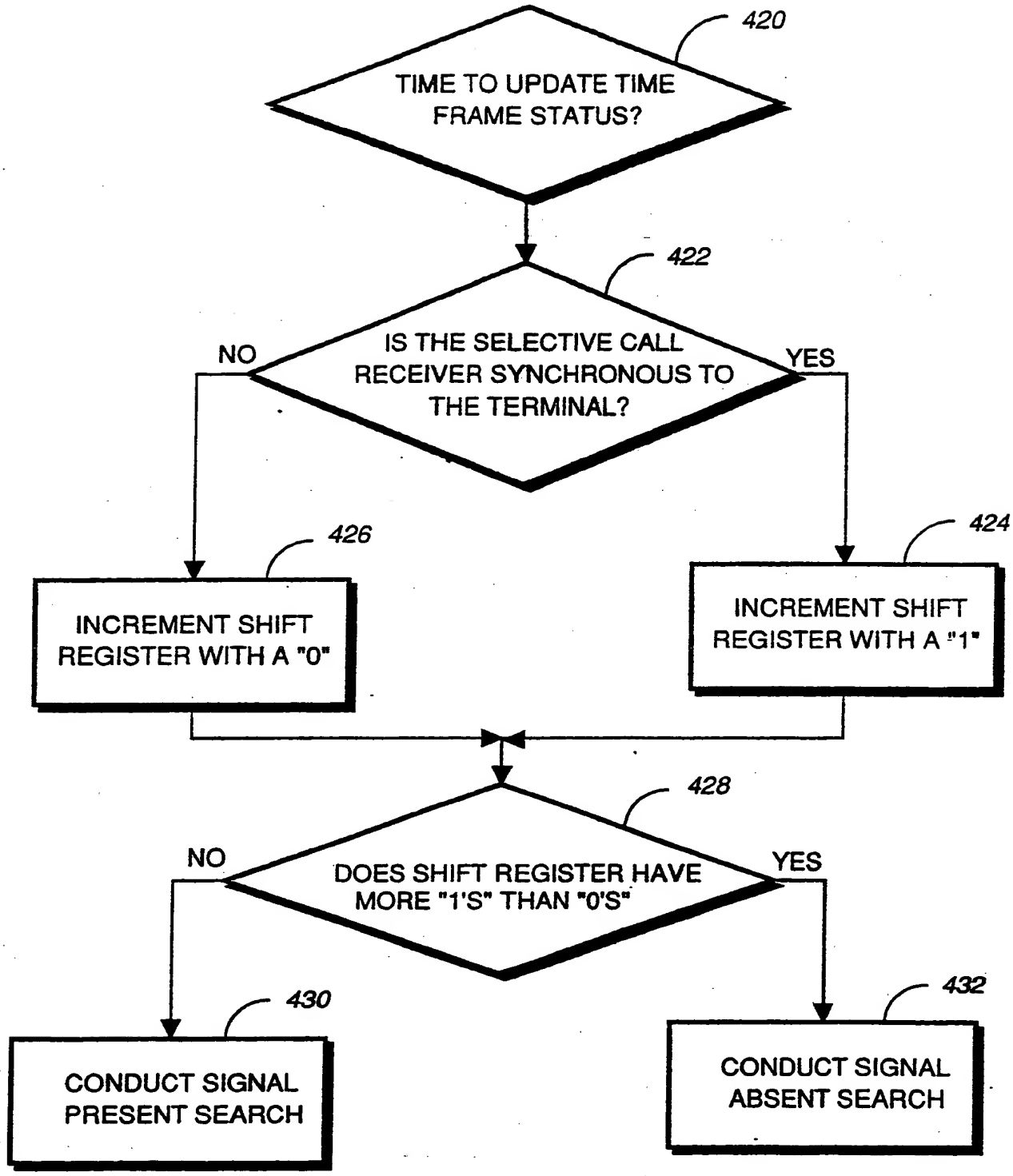
420
TIME TO UPDATE TIME FRAME STATUS?
422
IS THE SELECTIVE CALL RECEIVER SYNCHRONOUS TO THE TERMINAL?
NO
YES
426
INCREMENT SHIFT REGISTER WITH A "0"
424
INCREMENT SHIFT REGISTER WITH A "1"
428
DOES SHIFT REGISTER HAVE MORE "1'S" THAN "0'S"
NO
YES
430
CONDUCT SIGNAL PRESENT SEARCH
432
CONDUCT SIGNAL ABSENT SEARCH

FIG. 17

INTERNATIONAL SEARCH REPORT

International Application No. PCT/US91/03304

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [6]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC(5): H04B 1/16 G08B 5/22
US CL.: 455/161, 343

II FIELDS SEARCHED

Minimum Documentation Searched [7]

Classification System	Classification Symbols
U.S.	455: 89, 90, 161, 166, 343 340: 825.44, 825.47, 825.49

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [9]

Category *	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No. [13]
Y	US, A, 4,745,408 (NAGATA ET AL) 17 MAY 1988 SEE ENTIRE DOCUMENT	1-10
Y	US, A, 4,860,005 (DELUCA ET AL) 22 AUGUST 1989 SEE ENTIRE DOCUMENT	1-10
Y	US, A, 4,903,335 (SHIMIZU) 20 FEBRUARY 1990 SEE ENTIRE DOCUMENT	1-10

* Special categories of cited documents: [10]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search

27 JUNE 1991

Date of Mailing of this International Search Report

26 AUG 1991

International Searching Authority

ISA/US

Signature of Authorized Officer

NGOC-HO

for LISA CHAROUEL INTERNATIONAL DIVISION

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